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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/779,733	02/18/2004	Jung-Ho Lee	253/006 CIP 2	2084

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EXAMINER	
BERRY, RENEE R	

ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 06/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/779,733	LEE ET AL.	
	Examiner	Art Unit	
	Renee R. Berry	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 July 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-25 are rejected under 35 U.S.C. 102(e) as being anticipated by US Patent No.6,762,126 to Cho et al.

In regards to claim 1, Cho teaches a method of forming a silicon oxide layer in a semiconductor manufacturing process comprising: forming a planar spin on glass (SOG) layer by coating an SOG composition onto a semiconductor substrate having a stepped portion formed thereon; pre-baking the substrate at a temperature of from about 100 to about 500.degree C for about 1 to about 10 minutes; maintaining a loading temperature of a furnace into which the substrate will be loaded at about 500.degree. C. or less; loading the substrate into the furnace; and main-baking the substrate at a temperature of from about 500 to about 1200 degree C for about 10 to about 120 minutes to form a silicon oxide layer on the substrate at column 9, lines 62-67 and column 10, lines 16-25, claim 1.

In regards to claim 2, teaches the method as claimed in claim 1, further comprising

implementing an edge bead removal after forming the SOG layer.

In regards to claim 3, Cho teaches the method as claimed in claim 2, further comprising implementing a chemical mechanical polishing (CMP) process after forming the silicon oxide layer at column 11, lines 27-33, claim 20.

In regards to claim 4, Cho teaches the method as claimed in claim 1, wherein the substrate is pre-baked for about 4 to about 6 minutes at a temperature of from about 130 to about 230 degree C at column 6, lines 15-19.

In regards to claim 5, Cho teaches the method as claimed in claim 1, wherein the substrate is pre-baked under an atmosphere of air, an oxygen gas, moisture, a mixture of oxygen and moisture, a nitrogen gas or in a vacuum at column 8, lines 11-15.

In regards to claim 6, Cho teaches the method as claimed in claim 1, wherein the main-baking is implemented for about 30 to about 60 minutes at column 6, lines 20-25.

In regards to claim 7, Cho teaches the method as claimed in claim 1, wherein the substrate is main-baked under an atmosphere of air, an oxygen gas, moisture, a mixture of oxygen and moisture, a nitrogen gas or in a vacuum at column 6, lines 25-27.

In regards to claim 8, Cho teaches the method as claimed in claim 1, further comprising

increasing a temperature in the furnace by about 7.+-.3 degree C./min after loading the substrate into the furnace at column 6, lines 25-27.

In regards to claim 9, Cho teaches the method as claimed in claim 8, wherein the temperature of the furnace is increased under an atmosphere of air, an oxygen gas, moisture, a mixture of oxygen and moisture, a nitrogen gas or in a vacuum at column 6, lines 25-27.

In regards t claim 10, Cho teaches the method as claimed in claim 1, wherein the spin-on glass composition is a polysilazane-based spin-on glass composition at column 10, lines25-29, claim 2.

In regards to claim 11, Cho teaches the method as claimed in claim 10, wherein the spin-on glass composition comprises: from about 20 to about 30% by weight of perhydropolysilazane having a structure of --(SiH.sub.2NH).sub.n-- (in which n represents a positive integer), having an average molecular weight of from about 4,000 to about 8,000, and having a molecular weight dispersion degree of from about 3.0 to about 4.0; and from about 80 to about 70% by weight of a solvent at column 10, lines 33-37, claim 4.

In regards to claim 12, Cho teaches the method as claimed in claim 11, wherein the spin-on glass composition has a uniform viscosity of from about 1 to about 10 mPa at a

shear rate of from about 54 to about 420 (1/s) at column 10, lines 41-43, claim 6.

In regards to claim 13, Cho teaches the method as claimed in claim 11, wherein the spin-on glass composition has a contact angle of no more than about 4 degree with respect to an underlying layer on which the spin-on glass composition is to be coated at column 10, lines 44-46, claim 7.

In regards to claim 14, Cho teaches the method as claimed in claim 11, wherein the spin-on glass composition includes at least one compound including an element selected from the group consisting of boron, fluorine, phosphorous, arsenic, carbon and oxygen as an impurity material at column 12, lines 31-33, claim 26.

In regards to claim 15, Cho teaches the method as claimed in claim 11, wherein the solvent is xylene or dibutyl ether at column 7, lines 26-28.

In regards to claim 16, Cho teaches the method as claimed in claim 1, wherein a thickness of the silicon oxide layer is from about 4,000 to about 6,500 Angstroms at column 7, lines 16-19.

In regards to claim 17, Cho teaches the method as claimed in claim 1, wherein the stepped portion is formed by at least two conductive patterns at column 7, lines 54-55.

In regards to claim 19, Cho teaches the method as claimed in claim 17, wherein the two conductive patterns are gate electrodes or metal wiring patterns of a semiconductor device at column 7, lines 45-52.

In regards to claim 20, Cho teaches the method as claimed in claim 1, wherein an aspect ratio of the stepped portion is in a range of from about 5:1 to about 10:1 at Figure 10.

In regards to claim 21, Cho teaches the method as claimed in claim 1, wherein the stepped portion includes a closely stepped portion of which an aspect ratio is from about 5:1 to about 10:1 and a global stepped portion of which an aspect ratio is no more than about 1:1 at Figure 7.

In regards to claim 22, Cho teaches the method as claimed in claim 1, further comprising forming a silicon nitride layer having a thickness of from about 200 to about 600 .ANG. before coating the spin-on glass composition at column 10, lines 66-67, claim 13.

In regards to claim 23, Cho teaches a method of forming a silicon oxide layer in a semiconductor manufacturing process, comprising: forming a planar SOG layer onto a semiconductor substrate having a stepped portion formed thereon by coating an SOG composition comprising from about 20 to about 30% by weight of perhydropolysilazane

having a structure of --(SiH.sub.2NH).sub.n-- (in which n represents a positive integer), having a weight average molecular weight of from about 4,000 to about 8,000, and having a molecular weight dispersion degree of from about 3.0 to about 4.0, and from about 80 to about 70% by weight of a solvent; pre-baking the substrate at a temperature of from about 130 to about 230.degree. C. for about 4 to about 6 minutes; maintaining a loading temperature of a furnace into which the substrate will be loaded at about 500.degree. C. or less; loading the substrate into the furnace and increasing the temperature of the furnace by about 7.+-.3.degree. C./min; and main-baking the substrate at a temperature of from about 500 to about 1200.degree. C. for about 30 to 60 minutes to form a silicon oxide layer on the substrate at column 10, lines 16-66, claims 1-13.

In regards to claim 24, Cho teaches the method as claimed in claim 23, further comprising implementing an edge bead removal after forming the SOG layer, and implementing a CMP process after forming the silicon oxide layer at column 11, lines 27-33.

In regards to claim 25, Cho teaches the method as claimed in claim 23, wherein an aspect ratio of the stepped portion is in a range of from about 5:1 to about 10:1 at Figure 7.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Renee R. Berry whose telephone number is (571) 272-1774. The examiner can normally be reached on M-F 9-5:30.

The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

RRB
April 16, 2005

David Nelms
Supervisory Patent Examiner
Technology Center 2800